

Design and Implementation of an 8-bit Approximate Wallace Tree Multiplier for Energy Efficient Deep Neural Networks

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Abstract— Approximate arithmetic computing circuits and architectures have been proven to be energy efficient designs for Deep Neural Networks (DNNs) which are error resilient. In this paper, an approximate 8-bit Wallace Multiplier has been proposed and designed in 90nm CMOS technology for energy efficiency. The proposed 8-bit approximate multiplier design consumes ~32% less energy in comparison to an accurate 8-bit Wallace Tree multiplier with less than 20% Mean Relative Error (MRE).

Keywords— Approximate circuits, Energy Efficiency, Wallace Tree Multiplier, Deep Neural Networks, Ultra-low power.

I. INTRODUCTION

Deep Neural Networks have been demonstrated for variety of applications, including semantic segmentation, face detection, medical image recognition, and image/video processing. In order to produce accurate results, hardware architectures need to use more energy due to the large amounts of data and complex computations these applications involve [1]. Energy efficiency has become a crucial design requirement in the development of hardware for applications with limited resources, such as IoT nodes for edge computing. Therefore, architecture with ultra-low power consumption and high throughput or Energy-efficient circuits/architectures are high demand [2]. Most image/video processing applications are inherently error resilient. For such error resilient circuits/systems, approximate adders and multiplier designs have attracted wide interest [3-5].

Approximate computing is a popular computing technique that is used in systems do not require 100% accuracy [3] [4] [5]. By using approximate computing techniques, can achieve high speed, ultra-low power, and more energy efficiency. There are various levels to do approximations such as circuit-level approximation, logic level approximation, gate level approximation, and architecture level approximation [6][7].

In for image processing and video processing architectures, multiplication is the fundamental arithmetic operation that is frequently employed. Efficient multiplier design takes a key role in such applications [7]. In numerous applications for processing images and videos, multipliers come in different varieties. In such multipliers the Wallace Tree multiplier has been found to perform considerably faster execution compared to conventional multiplier due to the reduction in the number of stages [8] [9].

In this paper, we proposed a novel 8-bit approximate Wallace tree multiplier that reduces the consumption of area, energy, power, and delay.

The design and simulation are performed in Cadence 90nm CMOS technology and the synthesis reports demonstrate. the proposed 8-bit approximate multiplier design uses about 32% less energy, Compared to the accurate 8-bit Wallace Tree multiplier.

The rest of the paper is organized as. Section II. Demonstrates the state of the art in energy efficiency and approximate multipliers. Section III. Describes the Wallace tree multiplier design and operation; Section IV Presents the Wallace tree multiplier design and operation; Section V Analyze the results and analysis of the proposed multiplier design. Finally, conclusion is offered in Section VI.

II. STATE OF THE ART IN ENERGY EFFICIENT AND APPROXIMATE MULTIPLIER ARCHITECTURES

A. Traditional Multiplier Vs Wallace Tree Multiplier

An Efficient Multipliers should have the features such as Accuracy, Performance/Speed, Area, and Delay. In applications for processing images and videos, multipliers come in a variety of forms.

1. Booth Multiplier
2. Vedic Multiplier
3. Array Multiplier
4. Wallace Tree Multiplier.

When compared to conventional multipliers, Wallace tree Multiplier has high speed, because of reduction in critical path and adders. Wallace tree multiplier architecture uses less power and higher speed than other multiplier architectures [8-9]. Fig 1. depicts the basic block diagram of the Wallace Tree Multiplier, which consists of three blocks: 1. Partial product generation, 2. Partial product accumulation, and 3. Partial product addition.



Fig.1 Basic block diagram of Multiplier

Several Wallace tree multipliers works aimed at improving the performance of accurate arithmetic circuits have recently been proposed [9-13]. Wang et al [10] proposed non-volatile logic implementation using memristor-based MIG logic.

This method has been given the opportunity to research advanced processing designs in comparison to the traditional von Neumann Design. This approach has more memory bottleneck issues. Karuppusamy [11] proposed a fast and low forced multiplier with a high performance of the activity. In this article, a Baugh Wooley multiplier with a modified circuit is proposed for the rhythm virtuoso. The result was enhanced by the Baugh Wooley multiplier. Naveen Kumar et al [12] proposed a multiplier for calculation capacities where it is seen as more part in the electronics circuits. Depending on the multiplier investigation, this multiplier design KSA is recognized. This multiplier was used in several applications such as characterization of picture, video processing, and DSP. Mukherjee et al [13] presented a proposed counter based GDI Wallace tree multiplier that shows better outcomes with low utilization. The improvement is more for the higher number of bits. In order to increase the number of marked pieces, the Wallace tree multiplier can be used to replace the booth multiplier. The execution of such an on-chip multiplier is possible in various practical small-scale frameworks and MEMS processor units. Moreover, traditional multipliers are normally less energy efficient in the case of digital signal processors. Hence, finding an alternative way was a major concern at that time. In the case of Wallace Tree multipliers, we are using half adders, full adders, and a ripple carry adder for the reduction in the final stage. Many researchers tried to design simple techniques that showcased superiorities such as less power consumption, and high performance/speed, thus making them accordant in various implementations and applications in the field of electronics. Our primary goal is to design a process that will be acceptable for our needs. As the demand and development techniques keep improving, more and more complex systems need to be analyzed. So, we require a multiplier that has the advantage of satisfying our requirements. In order to achieve low energy and high performance, we proposed a Wallace tree multiplier that uses the fewest possible adders.

B. Some recent approximate Adder's, Multipliers:

Especially for Deep Neural Networks and Image Processing applications, approximate computing is one of the popular techniques for an energy-efficient architecture. Approximate computation will save a lot of energy by sacrificing precision. Instead of reducing accuracy, approximate computing gains from power consumption, area, and delay [14][23][24][25]. Approximate computing is very helpful in situations where accuracy is not as important.

Adders and Multipliers are approximated by using two methods, one is the General-purpose approximation method and the second one is the Problem-specific method. A few circuit groups, including adders and multipliers, can be approximated using general-purpose techniques. The structure of traditional adders and multipliers is exploited in problem-specific methods.

An approximate Adder and Multiplier is a basic arithmetic unit that is commonly used to reduce total energy consumption in many error-tolerant applications such as Deep Neural networks and Image Processing applications. [15][26],

An Approximate Multiplier based on the following several principles.

1. Using approximation to create partial products.
2. Through the exclusion of some incomplete products or the division of incomplete products into multiple modules.
3. implementing a rough compressor and counters in the partial product tree.

Lu [16] proposed a k -bit carry look-ahead adder in which only previous k bits are considered to estimate the current carry signal. Low probability of getting the right sum is shown by Lu's adder, which also increases area overhead. Shin et al. [17] reduce data-path delay and re-design the data-path modules. It eliminates the critical path in the carry-chain to take advantage of a certain error rate and increase parametric yield. Zhu et al. [18] [19] manifest an error-tolerant adder: ETA-I. ETA-I separates inputs into two categories: (1) Accurate parts, and (2) Inaccurate parts. No carry signal is taken into account in the latter at any bit position. Gupta et al. [20] target low-power and propose five different versions of mirror adder by reducing the number of transistors and internal node capacitance. Verma et al. [21] presented a Variable Latency Speculative Adder (VLSA) which provides approximate/accurate results but gives considerable delay and a large area overhead. Kahng et. al [22] proposed an accuracy reconfigurable adder with reduced critical-path and error rate.

C. Accuracy Design Metrics:

An approximate design with two n -bit inputs, A and B , each, where the exact results (P) and the approximate result (P'). The Accuracy Design Metrics are defined as follows [27] [28][29].

Error Rate (ER): When incorrect outputs are present in all outputs, it is also referred to as error probability.

Error Distance (ED): The mathematical difference between exact output and its approximative output for a given input data.

$$ED = |P - P'|$$

Relative Error Distance (RED): The proportion of accurate output to ED

$$RED = ED/P = |P - P'|/P$$

Mean Relative Error Distance (MRED): the average of every potential relative error distance.

Mean Square Error (MSE): It's described as being equal to the sum of the squared ED values.

III. WALLACE TREE MULTIPLIER

The multiplier architecture most frequently used in processors is the Wallace Tree Multiplier. The Wallace Tree architecture for multiplying two n -bit numbers consists of three steps.

1. partial product generation using several AND gates to multiply every bit of the multiplier with multiplicand.
2. Using full adders to decrease the sum of partial product multiplication (PPM).

- The partial product multiplication outputs from Phase 1 are grouped into sets of three rows, and the all sets are added with full adders. The sum and carry bits generated from the

$$\log_2 \frac{n^2}{4}$$


As we mentioned earlier there is a different approximating adder technique

All computing units are uses adders and multipliers, which are fundamental arithmetic circuits, in the hardware level. They can be used to significantly reduce energy consumption and speed up computations at the cost of a minimal accuracy loss. An 8-bit High Performance Approximate Wallace Tree Multiplier architecture for error- resilient and ultra-low power applications has been proposed in this work.

TOSAM, DSM and SAM are the different techniques to be introduced for approximation in accurate architectures in earlier works. In this work, we suggest a roughly designed multiplier that inspires a rough approximation of two of the three stages in the overall multiplication process. The final two stages one is the Reducing the sum of partial products by using full adders and second one is Generating Multiplication Results by Using 2-Input Addition are governed by the proposed approximation technique, as shown in Fig. 2. Initially, two 8-bit inputs are fed to approximate multiplier. PPM contains PPs which are generated using AND gates. After that, the PPMs rearrangement stage introduces the truncation method, and the final accumulation is carried out by combining a conventional ripple carry adder. After stage I is finished, the PPMs are created before the PPs are compressed and rearranged using full adder and half adder PPs. The number of full adders and half adders have been needed for compression is reduced with the rearrangement of PPs. Due to the fact that our suggested multiplier design uses two 8-bit inputs, it also contains an approximation of a full adder and a half adder for computing 8-bit multiplication.

A. Logic formulation in Approximating the Half-Adder Circuit:

The basic gate-level circuit diagram of accurate half adder as shown in Fig.3 and wave forms are describe in Fig.4

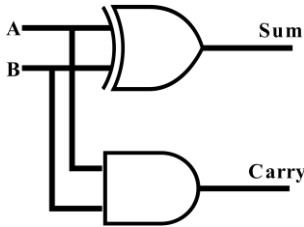


Fig.3 Gate Circuit of Half-Adder

An approximate half adder is replacing OR gate in place of XOR gate as shown in Fig.5 and wave forms are describe in Fig.6, if the input bits A [i] and B [j], are in the combination of (0,0), (0,1), (1,0) then the resulting sum is same as accurate half adder. Clearly, its values will be 0,1 and 1 respectively. On the other hand, A [i] and B [j] are in the combination of (1,1) then the sum cannot be determined accurately. In this condition, we observed that '1' is the error in sum as shown in Table.1

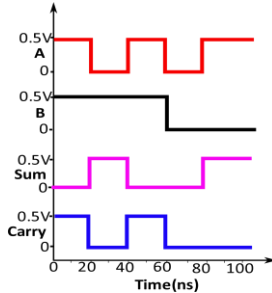


Fig.4 Accurate Half-Adder output wave forms

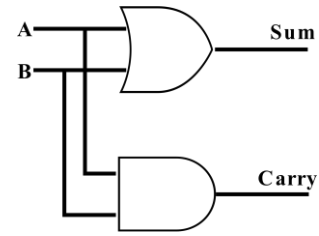


Fig.5 Gate Level Approximated Half-Adder

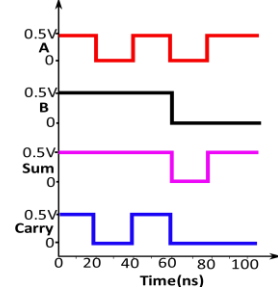


Fig.6 Approximate Half-Adder output wave forms

Table.1 Truth Table of Accurate and approximate Half adders

A	B	Accurate O/P Using XOR Gate		Approximate O/P Using OR Gate	
		Sum	C _{out}	Sum	C _{out}
0	0	0	0	0	0
0	1	1	0	1	0
1	0	1	0	1	0
1	1	0	1	1 X	1

B. Approximating the Full-Adder Circuit:

In this, we discuss how we can approximate a full adder circuit. We know that the full adder circuit is a combination of two adders. Basic gate-level circuit diagram and output waveforms of the full adder circuit as shown below in Fig.7 and Fig.8. By using the above approximation technique replace XOR with OR gate in the second half adder. The Approximating full adder circuit and output wave forms are as shown below in Fig.9 and Fig.10 from this approximation in full adder except for two conditions i.e., when A=0, B=1, C_{in}=1 and A=1, B=0, C_{in}=1 remaining all the conditions the approximate sum is equal to accurate sum as shown in Table 2.

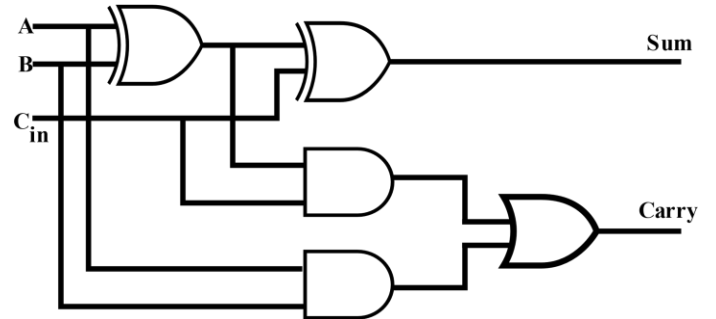


Fig.7 Gate Level Circuit of Full-Adder

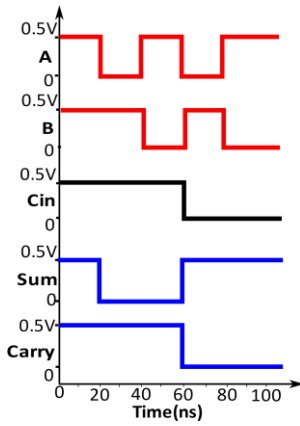


Fig.8 Accurate Full-Adder output wave forms

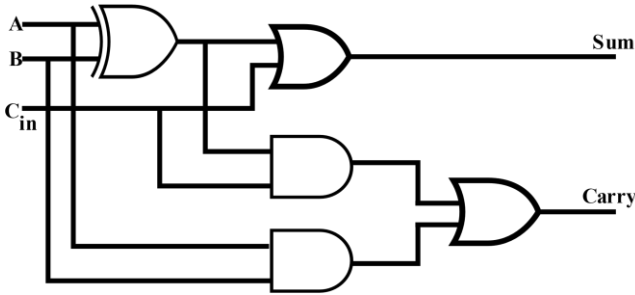


Fig.9 Approximate Full -Adder Circuit

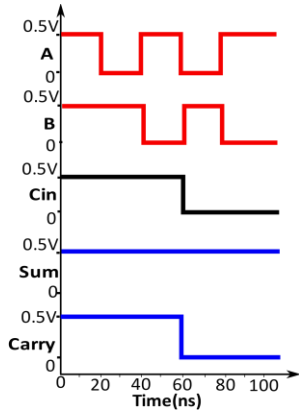


Fig.10 Approximate Full-Adder output wave forms

Table.2 Truth Table of Accurate and approximate Full adders

A	B	Cin	Accurate O/P Using XOR Gate		Approximate O/P Using OR Gate	
			Sum	C _{out}	Sum	C _{out}
0	0	0	0	0	0	0
0	0	1	1	0	1	0
0	1	0	1	0	1	0
0	1	1	0	1	1X	1
1	0	0	1	0	1	0
1	0	1	0	1	1X	1
1	1	0	0	1	0	1
1	1	1	1	1	1	1

C. Approximating the Wallace Tree Multiplier:

A 4x4 Wallace Tree Multiplier, a Ripple Carry Adder, a Full Adder, and a Half Adder are all included in the Wallace tree multiplier circuit. For designing of accurate 8-bit multiplier, we require a total of 85 standard cells (i.e Ripple Carry Adder, Full-Adder, Half-Adder), after approximating the 8-bit Wallace Tree Multiplier can reduce the total number of standard cells from 85 to 64. In this approximate technique, we can achieve a smaller mean relative error (MRE) Approximately less than 5%. Finally using this technique, we can achieve energy efficient 8-bit Wallace tree multiplier, what parameter got benefit will discuss in the next section.

V. RESULTS AND DISCUSSION

In this section we will discuss about power, speed, and area analysis for accurate and approximate circuits.

Half-Adder: The Approximate half-adder can achieve a 34.44% Reduced rate of energy consumption as compared with accurate half-adder. Table .3 shows the parametric analysis for Accurate and Approximate Half-Adder.

Table.3 Parameter analysis for Accurate and Approximate Half-Adder

Parameter	Accurate Half Adder	Approximate Half Adder
Power (uW)	1.826	0.711
Delay (nS)	0.034	0.031
Energy (aJ)	124.1	42.71
Reduced Rate of Energy Consumption (%)	34.44	

Full-Adder: The Approximate Full-Adder Can Achieve a 38.90% reduced rate of energy consumption as compared with accurate full adder. Table .4 shows the parametric analysis for Accurate and Approximate Full-Adder.

Table.4 Parameter analysis for Accurate and Approximate Full-Adder

Parameter	Accurate Full-Adder	Approximate Full-Adder
Power (uW)	4.518	3.774
Delay (nS)	0.0588	0.0274
Energy (aJ)	531.3	206.8
Reduced Rate of Energy Consumption (%)	38.9	

8-bit Wallace Tree Multiplier Performance metrics and Error Analysis:

The detailed synthesis report was generated using the genus tool, using this tool can generate a timing, power, and area report. Table.5 shows Performance Comparison of Accurate and Approximate 8-bit Wallace Tree Multiplier in terms of power, speed, and energy efficient. The Approximate Wallace Tree Multiplier Can Achieve a 75.52% reduced rate of power consumption as compared with accurate Wallace Tree

Multiplier as shown in below fig.11. The Approximate Wallace Tree Multiplier Can Achieve a 1.32x higher speed as compared with accurate Wallace Tree Multiplier as shown in below fig.12. and finally, The Approximate Wallace Tree Multiplier Can Achieve a 28.4% reduced rate of energy consumption as compared with accurate Wallace Tree Multiplier as shown in below Fig.13

Table 5: Performance Comparison of Accurate and Approximate 8-bit Wallace Tree Multiplier.

Parameter	Accurate Multiplier	Approximate Multiplier
Number of std cells	85	64
Area (μm^2)	387	291
Leakage Power (μW)	2.07	1.58
Dynamic Power (μW)	7.5	5.67
Total Power (μW)	9.6	7.25
Delay (nS)	110	83
Energy (pJ)	2.112	0.602
% MRE	0	20

Table 6. Presents the Implementation results of accurate and approximate 8-bit Wallace tree multiplier and it presents an error analysis for approximate 8-bit Wallace tree multiplier in terms of Error Distance (ED), Relative Error Distance (RED), Mean Relative Error Distance (MRED), and Mean Square Error (MSE). the Mean Relative Error is less than 20%.

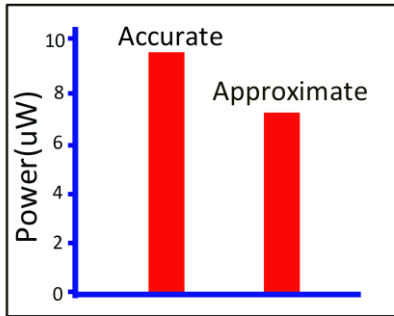


Fig 11. Power Analysis of 8-bit Wallace Multiplier

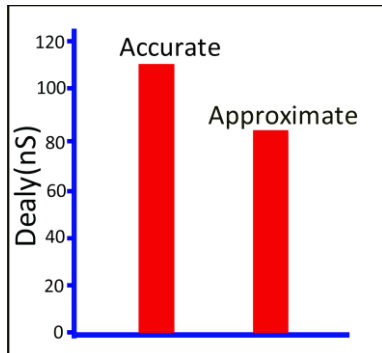


Fig 12. Delay Analysis of 8-bit Wallace Multiplier

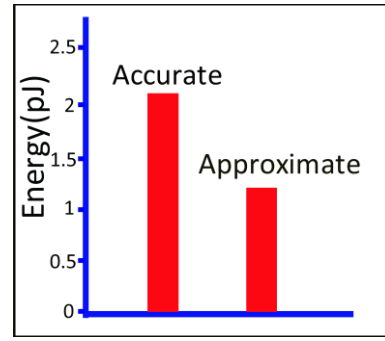


Fig 13. Energy Analysis of 8-bit Wallace Multiplier

Table 6. Error Analysis for 8-bit Wallace Tree Multiplier

A	B	Acc. O/P	Appr. O/P	ED	RED	MRED	MSE
10	10	100	116	16	0.16	0.0002	0.3906
17	17	289	305	16	0.0553	8.45E-05	0.3906
21	21	441	477	36	0.0816	0.000125	1.9775
25	25	625	697	72	0.1152	0.000176	7.9101
29	29	841	957	116	0.1379	0.00021	20.532
33	33	1089	1121	32	0.0293	4.48E-05	1.5625
37	37	1369	1405	36	0.0262	4.01E-05	1.9775
41	41	1681	1785	104	0.0618	9.44E-05	16.503
44	44	1936	2032	96	0.0495	7.57E-05	14.0625
49	49	2401	2417	16	0.0066	1.02E-05	0.3906
Average:					0.0723	0.000105	6.56969

VI. CONCLUSION

In this paper, an approximate 8-bit Wallace Multiplier has been proposed and designed in 90nm CMOS technology for energy efficiency. The proposed 8-bit approximate multiplier design consumes 75.52% lower power consumption and ~32% less energy in comparison to an accurate 8-bit Wallace Tree multiplier respectively with less than 20% Mean Relative Error (MRE), making it suitable for error resilient applications such as DNN accelerator architectures.

REFERENCES

- [1] Nojehdeh, M. E., Aksoy, L., & Altun, M. (2020, July). "Efficient Hardware Implementation of Artificial Neural Networks Using Approximate Multiply-Accumulate Blocks". In 2020 IEEE Computer Society Annual Symposium on VLSI (ISVLSI) (pp. 96-101). IEEE.
- [2] Seo, H., Yang, Y. S., & Kim, Y. (2020). Design and Analysis of an Approximate Adder with Hybrid Error Reduction. Electronics, 9(3), 471.
- [3] Jiang, H., Santiago, F. J. H., Mo, H., Liu, L., & Han, J. (2020). Approximate Arithmetic Circuits: A Survey, Characterization, and Recent Applications. Proceedings of the IEEE, 108(12), 2108-2135.
- [4] Prabakaran, B. S., Mrazek, V., Vasicek, Z., Sekanina, L., & Shafique, M. (2020, July). Approx-FPGAs: embracing ASIC-based approximate arithmetic components for FPGA-based systems. In 2020 57th ACM/IEEE Design Automation Conference (DAC) (pp. 1-6). IEEE.
- [5] Gupta, V., Mohapatra, D., Park, S. P., Raghunathan, A., & Roy, K. (2011, August). IMPACT: IMPrecise adders for low-power approximate computing. In IEEE/ACM International Symposium on Low Power Electronics and Design (pp. 409-414). IEEE.
- [6] Mrazek, V., Hrbacek, R., Vasicek, Z., & Sekanina, L. (2017, March). Evoapprox8b: Library of approximate adders and multipliers for circuit

- Automation & Test in Europe Conference & Exhibition (DATE), 2017 (pp. 258-261). IEEE.
- [7] Ullah, S., Rehman, S., Shafique, M., & Kumar, A. (2021). High-Performance Accurate and Approximate Multipliers for FPGA-based Hardware Accelerators. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*.
- [8] Kaushik, V., & Saini, H. (2017). A Review on Comparative Performance Analysis of Different Digital Multipliers. *Advances in Computational Sciences and Technology*, 10(5), 1257-1272.
- [9] Soniya, S. K. (2013). A review of different type of multipliers and multiplier-accumulator unit. *International Journal of Emerging Trends & Technology in Computer Science (IJETTCS)*, 2(4), 364-368.
- [10] Y. Wang et al., "A Few-Step and Low-Cost Memristor Logic Based on MIG Logic for Frequent-Off Instant-On Circuits in IoT Applications," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 4, pp. 662-666, April 2019, doi: 10.1109/TCSII.2018.2882388.
- [11] Karuppusamy, P. (2019). Design and analysis of low power. high-speed baugh wooley multiplier. *Journal of Electronics*, 1(02), 60-70.
- [12] Praveen Kumar, Y. G., Kariyappa, B. S., Shashank, S. M., & Bharath, C. N. (2020). Performance Analysis of Multipliers Using Modified Gate Diffused Input Technology. *IETE Journal of Research*, 1-13.
- [13] Waters, R. S., & Swartzlander, E. E. (2010). A reduced complexity wallace multiplier reduction. *IEEE transactions on Computers*, 59(8), 1134-1137.
- [14] Zervakis, G., Saadat, H., Amrouch, H., Gerstlauer, A., Parameswaran, S., & Henkel, J. (2021, January). Approximate Computing for ML: State-of-the-art, Challenges and Visions. In *2021 26th Asia and South Pacific Design Automation Conference (ASP-DAC)* (pp. 189-196). IEEE.
- [15] Chung, Y., Cho, M., & Kim, Y. Comparison of Hardware Accelerator of Matrix Multiplication with Approximate Adders. In *2021 International Conference on Electronics, Information, and Communication (ICEIC)* (pp. 1-2). IEEE.
- [16] Seok, H., Seo, H., Lee, J., & Kim, Y. (2021). COREA: Delay-and Energy-Efficient Approximate Adder Using Effective Carry Speculation. *Electronics*, 10(18), 2234.
- [17] Camus, V., Cacciotti, M., Schlachter, J., & Enz, C. (2018). Design of approximate circuits by fabrication of false timing paths: The carry cut-back adder. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, 8(4), 746-757.
- [18] hu, N., Goh, W. L., Wang, G., & Yeo, K. S. (2010, November). Enhanced low-power high-speed adder for error-tolerant application. In *2010 International SoC Design Conference* (pp. 323-327). IEEE.
- [19] Zhu, N., Goh, W. L., & Yeo, K. S. (2009). An enhanced low-power high-speed adder for error.
- [20] Gupta, V., Mohapatra, D., Park, S. P., Raghunathan, A., & Roy, K. (2011, August). IMPACT: IMPrecise adders for low-power approximate computing. In *IEEE/ACM International Symposium on Low Power Electronics and Design* (pp. 409-414). IEEE.
- [21] Verma, A. K., Brisk, P., & Ienne, P. (2008, March). Variable latency speculative addition: A new paradigm for arithmetic circuit design. In *Proceedings of the conference on Design, automation, and test in Europe* (pp. 1250-1255).
- [22] Kahng, A. B., & Kang, S. (2012, June). Accuracy-configurable adder for approximate arithmetic designs. In *Proceedings of the 49th Annual Design Automation Conference* (pp. 820-825).
- [23] J. Han and M. Orshansky, "Approximate computing: An emerging paradigm for energy-efficient design," 2013 18th IEEE European Test Symposium (ETS), Avignon, 2013, pp. 1-6, doi: 10.1109/ETS.2013.6569370.
- [24] B.Sivaranjani , R.Krishnaveni , P.Sakthy Priya , M.Sathishkumar, I.Vivek Anand, 2020, Design of Low Power Multiplier Unit using Wallace Tree Algorithm, *INTERNATIONAL JOURNAL OF ENGINEERING RESEARCH & TECHNOLOGY (IJERT)* Volume 09, Issue 02 (February 2020).
- [25] An Area Efficient Wallace Tree Multiplier using Modified Full Adder. (2020). *International Journal of Recent Technology and Engineering*, 8(6), 3383-3386. <https://doi.org/10.35940/ijrte.f8814.038620>
- [26] Smruthi Koushika Ravindran, Krishna Anand, Vigneswaran T, Ravi V, "High Performance Design of Wallace Tree Multiplier using Hybrid Adders", *IJAST*, vol. 29, no. 6s, pp. 4142 -, Jun. 2020.
- [27] Masadeh, M., Hasan, O., & Tahar, S. (2019). Error analysis of approximate array multipliers. *arXiv preprint arXiv:1908.01343*.
- [28] S. Arya N, "Approximate Computing: A New Trend in VLSI Based Multipliers for Error Resilient DIP Applications," *International Research Journal of Engineering and Technology*, Apr. 2018, www.irjet.net/archives/V5/i4/IRJET-V5I4864.pdf.
- [29] Bhardwaj, K., Mane, P. S., & Henkel, J. (2014, March). Power-and area-efficient approximate wallace tree multiplier for error-resilient systems. In *Fifteenth International Symposium on Quality Electronic Design* (pp. 263-269). IEEE.